DESIGN TECHNIQUES & CONSIDERATIONS FOR MULTILAYER PCB LAYOUT

23 NOVEMBER 2018
NANYANG POLYTECHNIC
• **Printed Circuit Board**

• PCB is the heart & soul of all electronic, telecommunication, microelectronic, satellite, medical, military products

• Interface for hardware, software and firmware

• Testbed platform for smart devices and future technology
• IoT devices will involve PCB design incorporating
  ✓ NB-IoT microchips
  ✓ LAN networks
  ✓ RF interface
  ✓ other electronic devices
OBJECTIVES

• To understand the PCB design process

• To get to know the industry standards for PCB design

• To explore the techniques and considerations for PCB design
DESIGN FLOW PROCESS

- Schematic Library Creation
- Capacitor
- Inductor
- LED
- Crystal
- Resistor
- Diode
- Quad Gate IC
Design Flow Process

Schematic Library Creation → Schematic Capture
DESIGN FLOW PROCESS
Design Flow Process

1. Schematic Library Creation
2. Schematic Capture
3. Footprint Creation
DESIGN FLOW PROCESS

2-pin small components

- Inductor
- Capacitor
- LED
- Resistor
- Diode
2-pin capacitor
DESIGN FLOW PROCESS

8-pin SOIC

Offset Null 1
Inverting (−) 2
Non-Inverting (+) 3
(Power) V− 4

8 Not Connected (NC)
7 V+ (Power)
6 Output
5 Offset Null

#REFDES
DESIGN FLOW PROCESS

1. Schematic Library Creation
2. Schematic Capture
3. Footprint Creation
4. Board Creation
Design Flow Process

• Grid setup
• Units setup
• Board outline definition – workspace for PCB design
Design Flow Process:

1. Schematic Library Creation
2. Schematic Capture
3. Footprint Creation
4. Component Placement
5. Board Creation
DESIGN FLOW PROCESS
Design Flow Process

1. Schematic Library Creation
2. Schematic Capture
3. Footprint Creation
4. Component Placement
5. Board Creation
6. Routing
DESIGN FLOW PROCESS
DESIGN FLOW PROCESS

- Schematic Library Creation
- Schematic Capture
- Footprint Creation
- Component Placement
- Board Creation
- Routing
- Design Rule Check
Design Flow Process

• Checks for
  - placement or routing errors
  - short/open circuit connections
  - minimum copper-copper spacing & width
  - total routed lengths
  - length-matching (if any)
  - differential pair routing
DESIGN FLOW PROCESS

Schematic Library Creation -> Schematic Capture -> Footprint Creation

Routing <- Component Placement <- Board Creation

Design Rule Check <- Backend Process
**DESIGN FLOW PROCESS**

• Backend is the preparation work done before any output files are generated

• Intended for: customer, end-user, QA/QC checker, PCB manufacturer

• Comprises of any DFM/DFT/DFA (Design for Manufacturing/Testing/Assembly) feedbacks
Design Flow Process

• Involves work such as ....

  - Reference designators
Design Flow Process

- Involves work such as ....
  - Reference designators
  - Labels, logos, identification text/numbers, branding, manufactured dates
DESIGN FLOW PROCESS

• Involves work such as ....

- Reference designators
- Labels, logos, identification text/numbers, branding, manufactured dates
- Touchups/copper editing
DESIGN FLOW PROCESS

BEFORE

AFTER
DESIGN FLOW PROCESS

BEFORE

AFTER
Design Flow Process

- Involves work such as ....
  - Reference designators
  - Labels, logos, identification text/numbers, branding, manufactured dates
  - Touchups/copper editing
  - Title block
## DESIGN FLOW PROCESS

- **Title block**
  - Contains information pertaining PCB layout design
  - Standard Wizlogix title block
**Design Flow Process**

- Involves work such as ....
  - Reference designators
  - Labels, logos, identification text/numbers, branding, manufactured dates
  - Touchups/copper editing
  - Title block
  - Drill table/quantity
## DESIGN FLOW PROCESS

### DRILL CHART: TOP to BOTTOM

**ALL UNITS ARE IN MILS**

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<th>FINISHED_SIZE</th>
<th>TOLERANCE_DRILL</th>
<th>PLATED</th>
<th>QTY</th>
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DESIGN FLOW PROCESS

- Schematic Library Creation
- Schematic Capture
- Footprint Creation
- Routing
- Component Placement
- Board Creation
- Design Rule Check
- Backend Process
- Gerber Generation
DESIGN FLOW PROCESS

• Output file: 2D Binary Vector Image file

• 2 Major formats:
  - Extended Gerber or RS-274X (Current Gerber Format)
  - Standard Gerber or RS-274D (Obsolete format)

• Mainly used in fabrication and assembly house for translating into Phototools for image transfer or as an Assembly guide
DESIGN FLOW PROCESS

External Layer

Internal Layer

SS Layer

SM Layer

Drill Layer
OBJECTIVES

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PCB DESIGN

WHAT STANDARDS ???

IPC
INTRODUCTION TO IPC

IPC – Institute of Printed Circuits

Previously known as Association Connecting Electronics Industries

Founded in 1957

Strong foundation as technical organization dedicated to meeting industry needs

Focus on PCB Design, Manufacturing and Electronics Assembly
INTRODUCTION TO IPC

IPC Standards

• Represent the best practices for electronics industry

• Highly focused on needs of the electronic industry

• Contain information related to the entire supply chain, from materials (PCB) to final electronics assemblies (PCBA)

• These standards are developed through the consensus of industry, including IPC members, academics, government agencies, OEMs, OCM and IMS companies.
  - OEM – Original Equipment Manufacturer
  - OCM – Original Component Manufacturer
  - IMS – Intelligent Manufacturing Systems

• The IPC’s standards are used, recognised worldwide and participation is voluntary
INTRODUCTION TO IPC

IPC Classes

- Class 1 – General Electronic Products
  - Limited life-span product
  - Function of completed product required
  - Plug & Play products, consumer electronics etc.
INTRODUCTION TO IPC

IPC Classes

• Class 2 – Dedicated Service Electronic Products
  ➢ Continued performance, extended life required
  ➢ Uninterrupted service desired, not critical
  ➢ Basic medical service, automotive, construction etc.
INTRODUCTION TO IPC

IPC Classes

• Class 3 – High Reliability Electronic Products
  ➢ Continued high performance, performance-on-demand critical
  ➢ Uninterrupted service critical, no downtime allowed
  ➢ Critical medical service, military, satellite, telecommunications etc.
OBJECTIVES

• To understand the PCB design process

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• To explore the techniques and considerations for PCB design
PCB DESIGN

- Design for Testing (DFT)
- Design for Manufacturing (DFM)
- Design for Assembly (DFA)
DESIGN FOR MANUFACTURING (DFM)
1) Component Placement Planning

- Plan/Organise ahead where each component is to be placed on the design workspace
- Priority level 1: Critical
- Priority level 2: Intermediate
- Priority level 3: Discretes
1) Component Placement Planning

- Components carrying hi-speed/critical signals to be placed far from board, where possible
- Group logic families together as a functional group
1) Component Placement Planning

- Allow 3 - 5mm clearance around ICs (eg. BGA, PLCC, QFP, FPGA) to facilitate rework (solder/de-solder to replace faulty BGAs)

- Other component spacing should allow access for the tools designed for inspection, rework and repair
1) Component Placement Planning

- Check with Assembly House on their DFA (Design for Assembly) specifications
- Components should not be grouped in such a way that they shadow one another during soldering
2) Mechanical constraints
   - Consider special features such as
     - Mounting/alignment/tooling holes
     - Height constraint areas
   - Slots/grooves required for chassis
   - Height constraint areas
   - Slots/grooves required for chassis
   - Keepout areas for component/copper
   - Areas interfacing with other mechanical parts, (e.g. Motor, generator, moving parts, high frequency signals)
3) Routing Planning

- Crosstalk between sensitive & non-sensitive signals
  - Specify & control conductor-to-conductor spacing
  - Reduce GND separation for GND plane
Design for Manufacturing

3) Routing Planning

➢ Crosstalk between sensitive & non-sensitive signals
   - Place components closer to minimize routing lengths
   - Restrict conductor parallelism, where possible

- Add GND separation with vias, where possible
4) Thermal Management
   - Easily heated components shall be spaced apart as greatly as possible
4) Thermal Management

- Convection cooling-components shall be placed such that air flows parallel to component orientation.
- Conduction cooling usually involves the placement of a metal ‘heat sink’ or ‘chill plate’ on the surface or buried within the board.
- In these applications, placement must allow for sufficient metal surface area (i.e., usually requires greater component spacing).
5) Layer Stackup

➢ 2 Layers, 4 Layers or more

➢ More layers = Higher cost
5) Layer Stackup

- 2 Layers, 4 Layers or more
- More layers = Higher cost

10 Layers
5) Layer Stackup

➢ Makeup of the internal structure
  ❑ Copper foil
  ❑ Prepreg layer
  ❑ Core material
  ❑ Soldermask
  ❑ Silkscreen
DESIGN FOR TESTING (DFT)
Design for Testing

• Fabricated PCB boards are subjected to electrical testing

- To monitor the connectivity state of the PCB, using capacitance & resistance tests
- Capacitance test will check for shorts/opens
- Resistance test will measure the conductor resistance using current (i.e., low resistance = good conductor)
**Design for Testing**

- 2 types of electrical testing
  - **Flying Probe**
    - Probes moving all across a PCB
  - **Testjigs**
    - Using fixture with fixed probes to test specific points on a PCB
Design for Testing

- Manual testing
  - Using multimeter to test point to point readings
• Testpoints (Probe points) are added within a PCB design
  ➢ A round copper pad
  ➢ Round plated hole
  ➢ Test turret
Design for Testing

• Testpoints are added within a PCB design to aid in electrical testing

  Round copper pads
    ➢ Spread out all over PCB design
    ➢ Either 1 or 2 sided
    ➢ Good for flying probe, testjig & manual testing
    ➢ Cost-saving, no additional component
Design for Testing

- Testpoints are added within a PCB design to aid in electrical testing

Round plated holes / Test turrets
- Usually only on 1 side
- Good for manual testing by clips, probe wires
- Additional cost due to fixture/component
Design for Testing

- Probe pins type
PCB DESIGN

- DESIGN FOR MANUFACTURING (DFM)
- DESIGN FOR TESTING (DFT)
- DESIGN FOR ASSEMBLY (DFA)
DESIGN FOR ASSEMBLY
(DFA)
Design for Assembly

• Components vs Board edge
  ➢ All components are to maintain a safe distance from the edges
  ➢ Main purpose: Facilitate mechanical assembly/handling/testing process
  ➢ Prevent components fallout at assembly/packaging/transporting stage
  ➢ All with the exception of Mechanical-specific components (ie. Connectors)
    ❑ Inputs from ME/R&D EE on connector location
    ❑ Cable length/direction of cable mount/connector contact points
    ❑ Protrusion of connectors in regards to chassis body
    ❑ Other movable parts surrounding PCB (eg. Motor belts, shaft pins, rotating objects....)
Design for Assembly

- Components vs Board edge
  - Ease usage of clamps/rails for holding PCB in place
  - For rails, a keepout area of 5mm is required on 2 sides
GERBER TECHNIQUES
GERBER TECHNIQUES

• Improvements made to alleviate potential manufacturing issues/defects during & after fabrication stage

• Upgrade overall look of the PCB
  • Cosmetic
  • Rework
  • Manual assembly

• Reduce time in correcting errors at the gerber stage
GERBER TECHNIQUES

Inconsistent plane separation gaps

Before: Soldermask opening opening smaller than copper pads

After: Soldermask opening opening smaller than copper pads
GERBER TECHNIQUES

Missing Soldermask/Pastemask areas

Silkscreen fall on copper areas
Gerber Techniques

- Gerber checks are usually done by the QC/QA team to ensure zero/minimal issues on PCB design.

- Gerber files can be viewed using CAM350, GraphiCode, GC Prevue, and Viewmate.
COURSES BY WIZLOGIX
UPCOMING COURSES

Break new ground with
Architecture and
System Design of NB-IoT
Transceivers

The Internet of Things (IoT) has been receiving a lot of attention in recent years. Despite the hype, the market has been slow to develop. Billions of devices are already connected to the internet, but as a quiet IoT revolution happens in the background, billions more are becoming accessible.

Stay ahead of the curve with Wizlogix

Time: 9:00 am-5:00 pm
Lunch and tea breaks refreshments are provided
Registration starts at 8:30 am
Location: Singapore
Register Now

Upcoming course date:
25 – 29 March 2019

Who Should Attend?

- RFIC and analog circuit design engineers, researchers and graduate students who are interested in higher level system and architecture design
- Electronic engineers who want to move into the IoT field and communication transceiver design
- Technical managers, marketing engineers and marketing managers who want to understand NB-IoT

Course Outline

Day 1:
What is NB-IoT?
- Introduction
- Cellular standards
- Differences in NB-IoT to other cellular standards

Transceiver Architecture
- Overview
- Heterodyne, LIF and ZIF receivers
- Heterodyne and direct up-conversion transmitters
- Constant envelope transmitters

Day 2:
Receiver Specifications and Architecture Development
- High level receiver specifications
- Noise and noise breakdown
- Receiver block specification lab
- Linearity and filtering
- Octave filtering lab
- ZIF and LIF architectures and trade-offs
- AWR Rx system lab
- Rx architecture summary

Day 3:
Transmitter Specifications and Architecture Development
- High level transmitter specifications
- Linearity for transmitters
- Noise in transmitters
- AWR Rx system lab
- Introduction to linearization
- AWR and Octave PA linearization lab

Day 4:
RF Front-end, Transmit and Receive Block Development
- Overview of cellular RF front-end
- Half-duplex vs. full duplex
- Front-end switch design
- Overview of Cellular RF Front-end
- SAW vs. BAW vs FBAR
- Introduction to PA design

Day 5:
Synthesizer Specification
- Synthesizer basics
- Synthesizer frequency specifications
- Synthesizer timing specifications

More Info:
Key Concepts
- Cellular transceivers
- Receiver operation
- Transmitter operation
- Noise partitioning
- Linearity partitioning
- Architecture breakdown/specification
- Synthesizer specification/operation

Tools Used
- AWR
- Octave (or MATLAB if attendee has licence)
- Excel (Apache Open Office Calc or Google Sheets as alternatives)
Learning Outcomes (Competencies)

- Understand the basic operation of NB-IoT
- Know how to find and read 3GPP specifications
- Become familiar with transceiver and front-end architectures for NB-IoT
- Understand the requirements and derive key specifications for the receive function
- Develop an architecture for the receiver and understand the trade-offs involved
- Understand the requirements and derive key specifications for the transmit function
- Develop an architecture for the transmitter and understand the trade-offs involved
- Derive key frequency and timing specifications
- Develop synthesizer architectures to meet those requirements
- Understand front-end module specifications and trade-offs
- Use the design tools in the specification and development of transceiver architecture

Course Facilitator

Dr Malcolm H. Smith is a director of AnalogueSmith (S) Pte. Ltd., a Singapore-based design house that delivers RF and analogue-centric solutions with a focus on IoT sensor nodes. He has worked as an independent consultant in the semiconductor industry for over four years, and has over 25 years’ industrial experience delivering mixed-signal, analogue, RFIC and RF solutions.

Prior to AnalogueSmith, Dr Smith spent nine years at Amalfi Semiconductor, where he designed CMOS power amplifiers and front-ends for cellular applications. While there, Dr Smith invented the output structure used on all Amalfi RFMD CMOS PAs, as well as the method to integrate the front-end switching in bulk CMOS for the World's first GSM/GPRS Tx Modules with integrated switch. He was also the lead of the group that designed a Band I WCDMA amplifier with the world-leading Figure Of Merit (FOM) for a CMOS PA of 80.
IPC COURSES

- IPC-A-600 Acceptability of Printed Boards
- IPC-A-610 Acceptability of Electronic Assemblies
- IPC/WHMA-A-620 Requirement & Acceptance for Cable & Wire Harness Assemblies
- IPC-6012 Qualification for Printed Boards
- IPC 7711/7721 Rework, Repair & Replace Printed Boards & Electrical Assemblies
- IPC J-STD-001 Requirement for Soldered Electronic Assemblies
- IPC Certified Interconnect Designers (CID)
- IPC Advanced Certified Interconnect Designers (CID+)
RESOURCE MATERIALS

• Eurocircuits – Full video on 4-layer PCB Fabrication
  https://www.youtube.com/watch?v=sIV0icM_Ujo